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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,246	10/31/2003	Harmeet Bhugra	5646-117	2284

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EXAMINER	
DOAN, DUC T	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,246	BHUGRA ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-24,27-43 and 46* is/are rejected.

7)☐ Claim(s) *4,5,25,26,44 and 45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-46 are in the application.

Claims 1-3,6-24,27-43,46 are rejected.

Claims 4-5,25-26,39,44-45 are objected to.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3,6-24,27-43,46 rejected under 35 U.S.C. 103(a) as being unpatentable over APA (US Application 10/698246) and in view of Malchior (US 6226710).

As for claim 1, APA describes an integrated search engine device, comprising: a content addressable memory (CAM) core that is configured to support at least one database of searchable entries therein (Fig 1: #36 cam core), and a control circuit that is configured to generate at least one signal at an output of the search engine device in response to detecting a done status of at least one of a plurality of result status signals that indicate states of completion of a

corresponding plurality of contexts being handled by the search engine device (Fig 1: #40 done bit for each context, APA's pages 1-2 describes a done bit that indicates the validity of the corresponding result value generated at the completion of each context. The result value is further stored in the respective result mailbox). Although APA does not describe the claim's aspect of one signal at an output of the search engine device. However, Melchior describes a similar CAM search engine that is capable of supporting both polling and interrupt driven architectures (Melchior's column 6, lines 38-45). Melchior's column 9 lines 54-60 further describes an interrupt pin on the CAM engine that can be used in interrupt driven architecture to cause an interrupt to occur when output data becomes available in the output FIFO. It would have been obvious to one of ordinary skill in the art at the time of invention to include the completion detection methods and structures as suggested by Melchior in APA's system to support multiple completion architectures such as polling or interrupt driven thus allowing for the flexibility to optimize the host interface architectures and to maximize the throughput of the CAM engine (Melchior's column 9 lines 38-42).

As for claim 2, APA describes wherein said CAM core and said control circuit are integrated on a common integrated circuit chip (APA's Fig 1 shows CAM cores #30, and control circuits are integrated in an IP co processor).

As for claim 3, the claim recites wherein the at least one signal comprises an interrupt. The claim rejected base on the same rationale as in the rejection of claim 1.

As for claim 6, APA describes wherein said control circuit further comprises a plurality of context specific result mailboxes that are configured to store return values associated with

corresponding ones of the plurality of contexts; and a result status register that is configured to store done status values associated with the plurality of contexts (APA's Fig 1: #40 mailbox).

As for claim 7, APA describes wherein the search engine device is configured to support a maximum number N of contexts, and wherein said result status register comprises N single-bit storage devices (APA's Fig 1: #40 shows a single valid bit for each context).

As for claim 8, APA describes wherein the search engine device further comprises a memory mapped interface that is coupled to an M-bit wide data bus; and wherein a value of N/M equals a positive integer greater than one (APA's Fig 1, pages 1-2 describes multiple contexts are sharing the same memory mapped interface)

Claims 9,17,27,30,46 rejected based on the same rationale as in the rejection of claim 6.

Claims 10,18,28,31 rejected based on the same rationale as in the rejection of claim 7.

Claims 11,19,29,32 rejected based on the same rationale as in the rejection of claim 8.

As for claim 12, the claim recites wherein said control circuit further comprises interrupt and non-interrupt indication circuits that are configured to receive the plurality of result status signals. The claim rejected based on the same rationale as in the rejection of claim 1. Melchior further describes circuits to support both interrupt driven and non-interrupt driven architectures (Melchior's column 9 lines 38-40).

As for claim 13, the claim recites wherein said control circuit further comprises a result status select register that is configured to store result status routing information that is provided to said interrupt and non-interrupt indication circuits. The claim rejected based on the same rational as in the rejection of claim 12. It has been known a CAM based search engine is

used to lookup routing address to forwarding a packet frame. In such application, the CAM lookup will results in routing information is provided.

Claim 14,20,22,33,35 rejected based on the same rationale as in the rejection of claim 12.

Claim 15,21,23,34,36 rejected based on the same rationale as in the rejection of claim 13.

Claims 16,24,37,40-42 rejected based on the same rationale as in the rejection of claim 1.

As for claim 38, Melchoir describes wherein said control circuit comprises a finite state machine (Melchoir's column 10 lines 25-35 describes the CAM engines executing commands with multiples sequence steps).

Claim 43 rejected based on the same rationale as in the rejection of claim 3.

Claim 39 rejected under 35 U.S.C. 103(a) as being unpatentable over APA (US Application 10/698246), Malchior (US 6226710) as applied to claim 37, and further in view of Henderson et al (US Pub 2002/0080789).

As for claim 39, the claim recites wherein said control circuit comprises a round robin scheduler and finite state machine. APA and Melchior do not describe the claim's aspect of a scheduler. However, Henderson describes a switch-based network device with a switch scheduler to schedule and processing elements being received at appropriated time (Henderson's Fig 3: #320, page 4 paragraph 29). As for the round robin aspect of the claim, it has been known in the art that in the situation of receiving multiple requests with the same priority consideration, the requests are schedule in a normal round robin fashion, in order to achieve a fair and equal scheduling of these requests. It would have been obvious to one of ordinary skill in the art at the time of invention to include the switch scheduler and structures as suggested by Henderson in

APA's system to resolve the execute order of multiple instructions, thereby allowing the device to executing several searching and packet modification simultaneously (Henderson's page 1 paragraph 13).

Allowable Subject Matter

Claims 4-5,25-26,44-45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

Claims 4-5 are allowable over the prior art of record because Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts which teach an integrated search engine device with a CAM core with result status signals corresponding to plurality of contexts being handled by the search engine and an aggregate result status signal an aggregate result status signal having a leading edge that is synchronized with a transition of a result status signal when the transition indicates completion of a first-to-finish one of the plurality of contexts being handled by the search engine device during overlapping time intervals (claim 4); combinational logic that is configured to maintain the aggregate result status signal in an active state so long as a value of any one of the plurality of result status signals indicates a state of completion of a respective one of the plurality of contexts (claim 5).

Claims 25-26,44-45 include the same novel features as those found in claims 4-5 as noted above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cheng (US 6629099) describes a parallel search engine.

Wanzakhade et al (US 6845024) describes a circuit to detect multiple matching.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin L. Ellis
Primary Examiner

Kevin L Ellis